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Ordinary Vector Network Analyzers Get Differential Port Measurement Capability

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This article describes a software-based method for obtaining differential measurements using a two-port unbalanced vector network analyzer

Yesterday's discrete RF circuits are rapidly becoming replaced with today's new RF integrated circuits (RFICs). In these new RFICs, differential or balanced ports are a common interface for transferring RF signal power into or out of the device, since balanced circuits can solve problems with grounding. The differential RF ports of these RFICs often need to be matched to the system impedance (typically 50 ohms), or some other balanced or unbalanced termination, for optimum performance or maximum power transfer.

The vector network analyzer (VNA) is an ideal instrument for measuring the complex impedance of the RFIC port and the load with which it will be terminated. When both the port and load impedances are accurately known then the matching network can be designed. However, many RF labs are equipped with a VNA that has only two unbalanced ports. The unbalanced VNA cannot directly measure the IC port or its termination if either one represents a balanced impedance.

The VNA with two unbalanced ports can be replaced with a new 4-port differential VNA, but this is an expensive solution costing tens of thousands of dollars. BALUNS are sometimes used as a low cost solution to interface a balanced circuit to the unbalanced port of a typical VNA instrument. This method has its drawbacks in time, effort and accuracy since the BALUN introduces errors as stray and parasitic impedances, and introduces issues of altered electrical length.

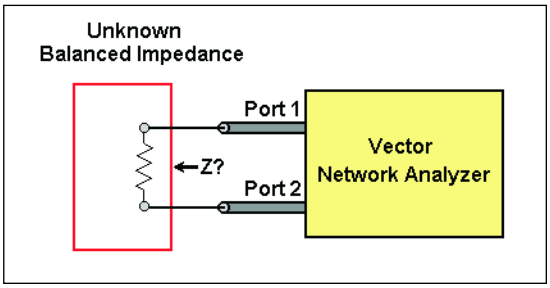


Figure 1 · Test configuration for making balanced measurements with an unbalanced vector network analyzer.

A Software Solution

LINC2 is a high performance, low cost (under US$500), RF and microwave circuit design and simulation program from Applied Computational Sciences. One of the unique features of LINC2's set of RF tools is its ability to turn a set of S-parameter measurements taken with an ordinary VNA into differential impedance data. This eliminates the need for introducing measurement BALUNS into the circuit and does not require an expensive differential VNA instrument. Moreover, LINC2 includes tools that utilize the differential impedance data by synthesizing balanced-to-balanced or balanced-to-unbalanced matching networks based on the data.

Figure 1 illustrates the test configuration for measuring a balanced impedance with an unbalanced VNA. The differential port or balanced impedance to be measured has two nodes above ground potential. The procedure is to apply each unbalanced port from the VNA to one side of the balanced port or impedance. The VNA is then calibrated to the point of contact with the circuit or the VNA's

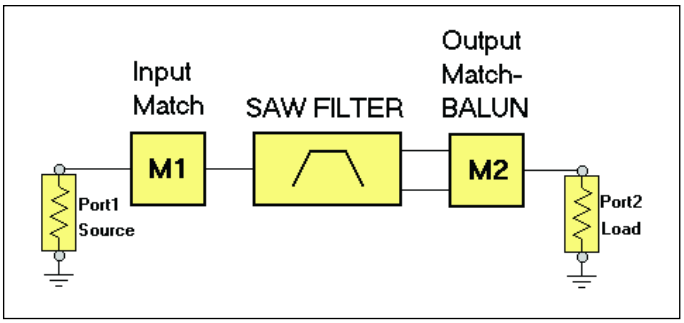


Figure 2 · SAW filter example.

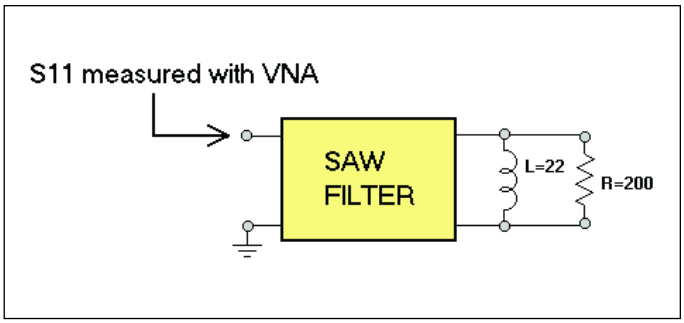


Figure 3 · Step 1: Input impedance measurement.

port extensions (or electrical delay feature) is used. Then, the full two-port S-parameter measurement is taken over the frequency range of interest (yielding four complex S parameters per frequency point). This data is then stored on floppy disk and transferred to a computer running the LINC2 program. LINC2 then transforms the VNA's S-parameter data into differential impedance data and displays it in a number of different formats. The data can be displayed as a linear differential reflection coefficient, a differential return loss in dB or as a complex differential impedance with real and imaginary parts.

Design Example—IF SAW Filter Matching

The receiver section of a CDMA cellular telephone, recently designed by the author, employed an IF SAW filter that required at least one port (two terminals) to be operated in a balanced configuration. The source and load circuits that would connect to the SAW filter were ultimately single ended, so a matching BALUN needed to be designed for one side of the filter. It was decided that a matching BALUN would provide the balanced load at the output side while the input side of the SAW filter would be matched with a single ended L match as shown in Figure 2.

Note that the output BALUN (M2) we are talking about here is part of the circuit and not a measurement device. The following procedure was used to design the input and output matching networks, M1 and M2:

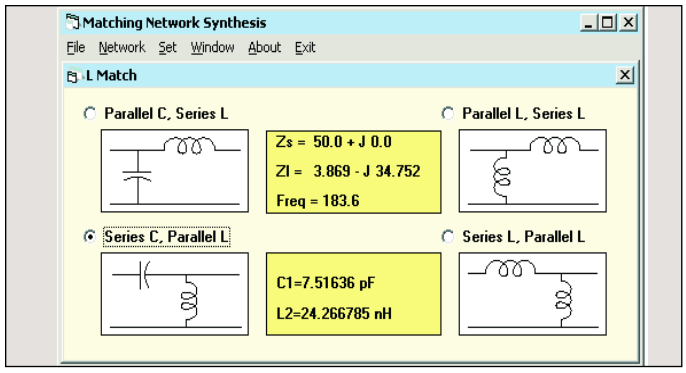


Figure 4 · Input matching network options.

Step 1—Determine the input impedance:

The input impedance of the SAW filter is determined by terminating the output terminals of the filter with the manufacturer's specified load impedance and then measuring the single-ended input impedance with a Vector Network Analyzer. The load impedance specified on the data sheet is only an approximation because it doesn't take into account the parasitic effects of the layout for the application circuit. However, any moderate amount of mismatch at the output will hardly be seen at the input because of the isolation provided by the filter's 10 dB of insertion loss. The manufacturer's data sheet for the CDMA SAW filter in Figure 2 calls for 200 ohms in parallel with a 23 nH inductor. The nearest standard value of 22 nH was used for the load inductor while the input reflection coefficient (S_{11}) was measured with a VNA as shown in Figure 3.

The measured S_{11} indicated an input impedance of 3.869 –j34.752 ohms.

Step 2—Design the input match:

Designing the matching network is easy with LINC2. Simply select the desired type of network from a list in the impedance matching tool and enter the source impedance (50 ohms), load impedance (3.869 –j34.752 ohms) and the operating frequency (183.6 MHz). LINC2's "Network" menu contains various forms of lumped and distributed (transmission line) matching networks. The L network was chosen for this example.

From the given impedance data, LINC2 computes all

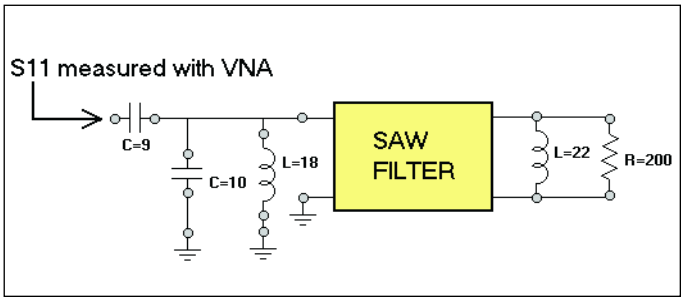


Figure 5 · Final input match after tuning.

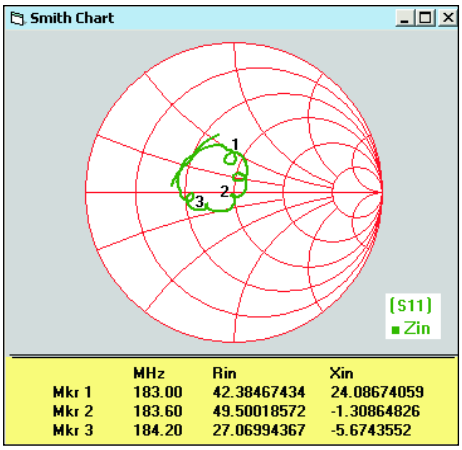


Figure 6 · Smith chart display of the input match.

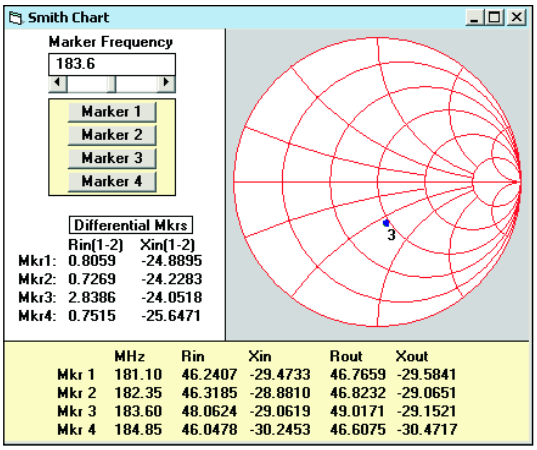


Figure 7 · Output impedance measurements, single-ended and differential.

the possible matching circuits and their component values. As shown in Figure 4, LINC2 automatically determines which circuit topologies are capable of solving the matching problem and makes only those selectable. In this case the high-pass network with a series C (7.52 pF) and shunt L (24.3 nH) was chosen. The series capacitor conveniently serves both as a matching element and as a coupling capacitor with DC blocking.

Step 3—Tune the input match:

Figures 5 and 6 show the input match after tuning the physical prototype circuit on the bench. All measurements were made using an Agilent 8753ES VNA. The first cut of the input circuit used a 10 pF capacitor in parallel with an 18 nH inductor to approximate the impedance of the 24.3 nH shunt inductor from Figure 4. Using an 8 pF capacitor for the 7.52 pF value suggested in Figure 4 resulted in an input impedance of 46 –j17 ohms. The resulting input return loss was quite good at nearly 15 dB. However, increasing the series input capacitor to 9 pF improved the input match to 49.5 –j1.3 ohms (Figure 6), yielding an input return loss greater than 37 dB at 183.6 MHz.

This completes the design of the input circuit (M1 in Figure 2). The next step is to design the output match (M2 in Figure 2). The goal was to design a lumped element BALUN that would provide a good output match without using transformers.

Step 4—Measure the output impedance:

In order to design the matching network, it is necessary to determine the differential output impedance of the SAW filter. This impedance is measured by connecting each port of the VNA to one of the two output terminals of the SAW filter as shown in Figure 1 and taking the two-port S-parameters while the input is properly terminated. The S-parameter file is then imported into LINC2 to produce the display in Figure 7. LINC2 displays the single-ended impedance (from each pin to ground) below the Smith chart and the differential impedance (between the pins) to the left of the chart.

The differential marker (Mkr3) at 183.6 MHz indicates a balanced output impedance of 2.84 –j24.05 ohms. The equivalent output impedance in parallel format is 206.5 ohms in parallel with a 35.5 pF capacitor. This agrees closely with the SAW filter's data sheet specification of the load impedance as 200 ohms in parallel with 23 nH (which corresponds to an output impedance of 200 ohms in parallel with 32.67 pF).

Ideally, a 22 nH inductor placed in shunt across the output terminals of the filter would resonate with the internal 35 pF capacitance and produce and output impedance of approximately 200 ohms resistive. However, any real inductor has loss which will effectively reduce the output impedance. Therefore, a more accurate measure-

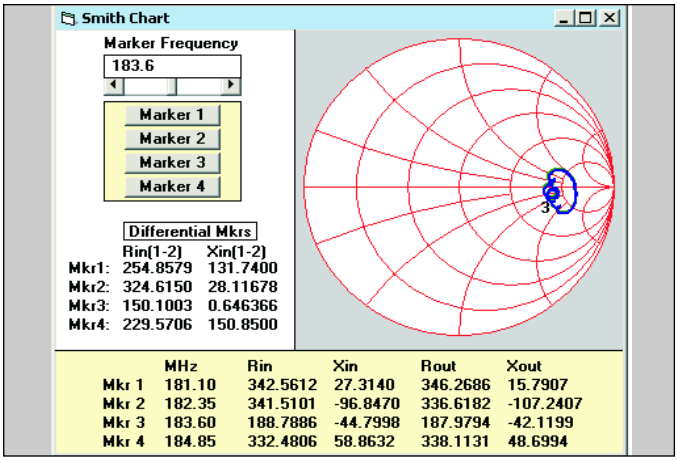


Figure 8 · Output impedance with shunt inductor.

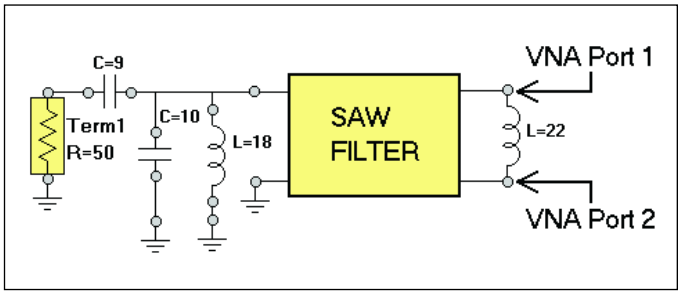


Figure 9 · Shunt inductor placed at output.

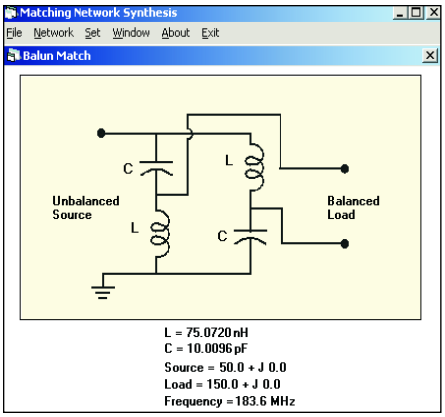


Figure 10 · Balanced-to-unbalanced matching network.

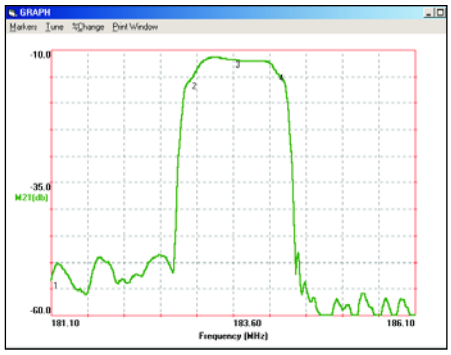
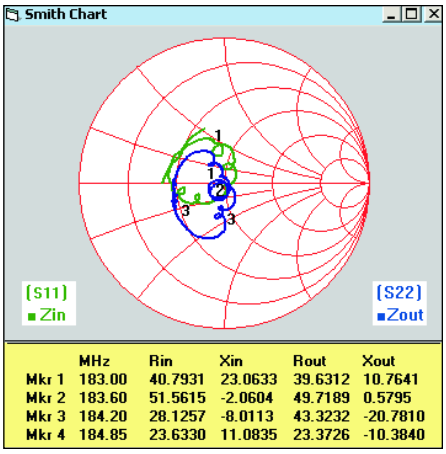


Figure 13 · Measured frequency response of the complete circuit.



	MHz	Rin	Xin	Rout	Xout
Mkr 1	183.00	40.7931	23.0633	39.6312	10.7641
Mkr 2	183.60	51.5615	-2.0604	49.7189	0.5795
Mkr 3	184.20	28.1257	-8.0113	43.3232	-20.7810
Mkr 4	184.85	23.6330	11.0835	23.3726	-10.3840

Figure 14 · Measured input and output match.

ment of the differential output impedance will be obtained by repeating the measurement with the inductor present at the output. Figure 8 displays the results of retaking the S-parameter measurement with the 22 nH inductor in shunt with the output as shown in Figure 9. As expected, the output impedance with the inductor present dropped while the reactance was effectively cancelled. Differential marker 3 in Figure 8 indicates a balanced output impedance of 150 ohms with less than one ohm of reactance at 183.6 MHz.

Step 5—Design the output matching circuit:

The differential output impedance of the SAW filter is 150.1 +j0.646 ohms. Selecting BALUN Match from the LINC2 network synthesis tool and entering 150 +j0 for the load impedance generated the lumped element circuit shown in Figure 10.

Figure 10 indicates that an unbalanced 50 ohm termination can be matched to the SAW filter's 150 ohm balanced output with two 75 nH inductors and two 10 pF capacitors in the configuration shown. The completed filter circuit is shown in Figure 11.

Step 6—Tune the output match:

Figure 12 shows the completed circuit as built and tested. Shunt 1.5 pF capacitors across standard 68 nH chip inductors replaced the 75 nH values in Figure 11. Using a smaller standard value inductor helped to compensate for parasitic capacitance in the physical inductors. The additional parallel capacitance (1.5 pF) provided a means to tune the circuit. After tuning, the best output return loss, passband and stop-band performance was achieved with the two 10 pF capacitors reduced slightly to 9.5 pF.

The measured frequency response of the complete filter circuit is shown in Figure 13. Figure 14 shows the quality of the input and output match (measured impedance). The measurements were taken with an Agilent 8753ES VNA. The network analyzer's data was imported and displayed using the LINC2 program.

The frequency response meets all specifications for insertion loss and out-of-band attenuation (rejection) listed in the filter's data sheet. The input and output match to 50 ohms at the band center are 51.6 –j2 and 49.7 +j0.58 ohms respectively. The input and output return loss remains better than –10 dB across the 1.2 MHz passband (183-184.2 MHz). This completes the CDMA IF filter design example.

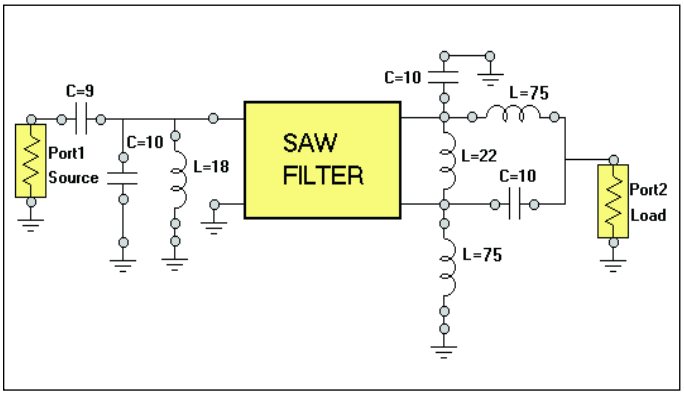


Figure 11 · Complete circuit, as designed.

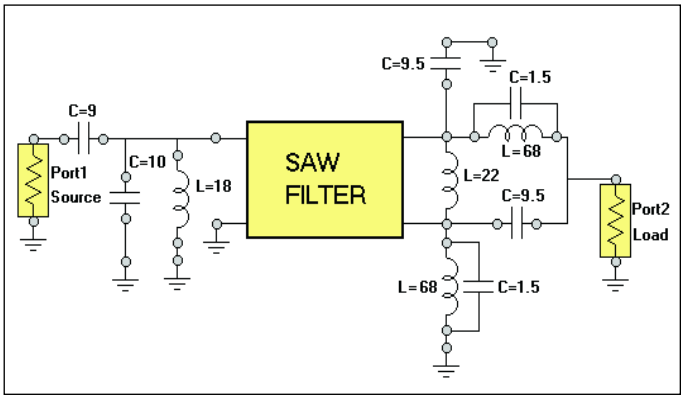


Figure 12 · Circuit after building and testing.

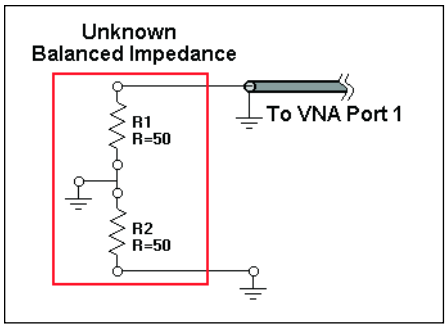


Figure 15 · Grounding one pin of a balanced port is an incorrect way to measure the impedance.

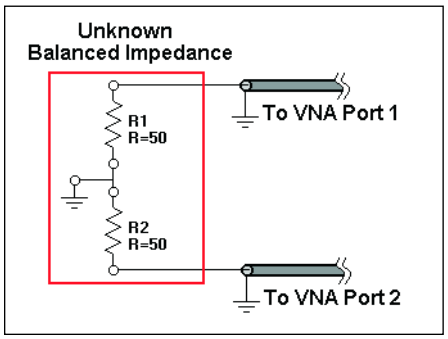


Figure 16 · Using both pins is required to obtain an accurate measurement.

Summary

Figure 15 depicts the danger of grounding one pin of a balanced port and attempting to measure the impedance from the remaining pin to ground. The result is that only half of the balanced impedance is measured.

Figure 16 shows the correct procedure as used in the CDMA filter design example above. If the unknown impedance is two 50 ohm center tapped resistors as shown, the first measurement (Figure 15) would yield 50 ohms, which is incorrect. The second measurement (Figure 16) extracts the two-port S-parameters and uses the LINC2 program to calculate and display the correct impedance, 100 ohms in this case.

Also note that with active circuits (RFICs), grounding an output pin can alter the internal ground reference and change circuit behavior.

Conclusion

LINC2 is a high performance linear RF and microwave simulation program with many value added features for automating design tasks, including circuit synthesis. This example showed how LINC2 can add differential port measurement capability to an existing vector network analyzer (with unbalanced ports) by post processing of the S-parameters. More information about LINC2 can be found on the company's web site.

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